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PATENT

Docket No. D-387

10/23/00
JC575 U.S. PTO

Commissioner of Patents and Trademarks
Washington, D.C. 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of

Inventor(s): Gee L. Lui and Kuang Tsai

For (title): Data Aided Symbol Timing Tracking System for Precoded Continuous
Phase Modulated Signals

JC575 U.S. PTO
09/696525
10/23/00

1. Type of Application

This new application is an ORIGINAL application.

2. Benefit of Prior U.S. Application(s) (35 USC 120) - No

CERTIFICATION UNDER 37 CFR 1.10

I hereby certify that this New Application Transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service on this date October 23 2000 in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number EK286601861US addressed to the: Commissioner of Patents and Trademarks, Washington, D.C. 20231

Carole A. Mulchinski

(Type or print name of person mailing paper)

Carole A. Mulchinski

(Signature of person mailing paper)

(Application Transmittal [4-1]--page 1 of 4)

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3. Papers Enclosed Which Are Required for Filing Date Under 37 CFR 1.53(b) (Regular) or 37 CFR 1.153 (Design) Application

26 Pages of specification
11 Pages of claims
1 Pages of Abstract
6 Sheets of drawing

☐ informal

☐ in triplicate

4. Additional papers enclosed

☐ Preliminary Amendment

☐ Information Disclosure Statement

☐ Form PTO-1449

☒ Small Entity Statement

5. Declaration or oath executed by INVENTOR(S)

☒ Enclosed

6. Inventorship Statement

The inventorship for all the claims in this application is THE SAME.

7. Language: ENGLISH

8. Assignment

☒ An assignment of the invention to The Aerospace Corporation
P. O. Box 92957 (M1/040), Los Angeles, CA 90009-2957

☒ is attached

☐ will follow

9. Certified Copy

attached Certified copy(ies) of application(s) X are not applicable are
 will follow.

10. Fee Calculation

☒ Regular application

CLAIMS AS FILED

Number Filed	Number Extra	Rate	Basic Fee
			\$710.00
Total Claims - 19 -20=	0	X \$ 9.00	
Independent Claims - 3 -3=	0	X \$ 40.00	00.00
Multiple dependent claim(s), if any		\$270.00	

☐ Amendment cancelling extra claims enclosed

☐ Amendment deleting multiple dependencies enclosed

☐ Fee for extra claims is not being paid at this time

Filing Fee Calculation

\$710.00

11. Small Entity Statement(s)

☒ Verified Statement(s) that this is a filing by a small entity under 37 CFR 1.9 and 1.27 is(are) attached.

\$355.00

12. Fee Payment Being Made At This Time

☐ No filing fee is to be paid at this time. (This and the surcharge required by 37 CFR 1.16(e) can be paid subsequently.)

☒ Enclosed

☒ Basic filing fee \$ 355.00

☒ Recording assignment (\$40.00; 37 CFR 1.21(h)(1)) \$ 40.00

Total fees enclosed \$ 395.00

(Application Transmittal [4-1]--page 3 of 4)

13. **Method of Payment of Fees**

☒ charge Account No. 01-0428 in the amount of \$ 395.00.
A duplicate of this transmittal is attached.

14. **Authorization to Charge Additional Fees**

☒ The Commissioner is hereby authorized to charge the following additional fees by this paper and during the entire pendency of this application to Account No. 01-0428.

☒ 37 CFR 1.16 (filing fees)

☒ 37 CFR 1.16 (presentation of extra claims)

☒ 37 CFR 1.16(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)

☒ 37 CFR 1.17 (application processing fees)

☒ 37 CFR 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 CFR 1.311(b)).

15. **Instructions As To Overpayment**

☒ credit Account No. 01-0428.

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☒ This transmittal ends with this page.

(Application Transmittal [4-1]--page 4 of 4)

Applicant or Patentee: Gee L. Lui, Kuang Tsai

Serial or Patent No.: _____

Filed or Issued: _____

For: Data Aided Carrier Phase Tracking System for Precoded Continuous Phase
Modulated Signals

**VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY
STATUS (37 CFR 1.9(f) and 1.27(d))--NONPROFIT ORGANIZATION**

I hereby declare that I am an official empowered to act on behalf of the nonprofit organization identified below:

NAME OF ORGANIZATION The Aerospace Corporation

ADDRESS OF ORGANIZATION P. O. Box 92957 (M1/040)

Los Angeles, CA 90009-2957

TYPE OF ORGANIZATION

☒ TAX EXEMPT UNDER INTERNAL REVENUE SERVICE CODE (26 USC
501 (a) and 501 (c) (3))

I hereby declare that the nonprofit organization identified above qualifies as a nonprofit organization as defined in 37 CFR 1.9(e) for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code with regard to the invention entitled Data Aided Carrier Phase Tracking System for Precoded Continuous Phase Modulated Signals

by inventor(s) Gee L. Lui, Kuang Tsai

described in

☒ the specification filed herewith

☐ application serial No. _____, filed _____.

I hereby declare that rights under contract or law have been conveyed to and remain with the nonprofit organization with regard to the above identified invention.

If the rights held by the nonprofit organization are not exclusive, each individual, concern or organization having rights to the invention is listed and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

I acknowledge the duty to file, in this application or patent, notification of any charge in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING Robert Donald Matthews

TITLE IN ORGANIZATION Assistant General Counsel

ADDRESS OF PERSON SIGNING The Aerospace Corporation

P. O. Box 92957 (M1/040), Los Angeles, CA 90009-2957

SIGNATURE

Robert Donald Matthews

DATE

October 20, 2000

PATENT APPLICATION

Docket No.: D387

Inventor(s): Gee L. Lui and Kuang Tsai

Title: Data Aided Symbol Timing Tracking System for Precoded
Continuous phase Modulated Signals

SPECIFICATION

Statement of Government Interest

The invention was made with Government support under contract
No. F04701-93-C-0094 by the Department of the Air Force. The
Government has certain rights in the invention.

Reference to Related Application

The present application is related to applicant's copending
application entitled Data Aided Carrier Phase Tracking System for
Precoded Continuous phase Modulated Signals, S/N: xx/xxx,xxx, filed
yy/yy/yy, by the same inventors.

1 Field of the Invention

2
3 The invention relates to the field of continuous phase
4 modulation communications systems. More particularly, the present
5 invention relates to symbol time tracking for continuous phase
6 modulations communications systems, such as Gaussian minimum shift
7 keying communications systems having small bandwidth time products.
8
9
10

11 Background of the Invention

12
13 In synchronous digital data communication systems, the carrier
14 phase and symbol timing of the received signal must be acquired and
15 tracked by the receiver in order to respectively demodulate the
16 received signal and to recover the transmitted data from the
17 received signal. Typically, receivers require carrier phase
18 tracking for signal demodulation and symbol time tracking for data
19 detection for generating received data streams.
20

21 Continuous phase modulation (CPM) provides a class of digital
22 phase modulation signals that have a constant envelope. The
23 spectral occupancy of a CPM signal can be controlled or tailored to
24 the available bandwidth of a transmission channel. The constant
25 envelope CPM signals allow saturated power amplifier operation for
26 maximum power efficiency. The use of CPM signals in communications
27 systems can potentially achieve significant improvement in both
28 power and spectral efficiency over other conventional modulation

1 techniques, at the cost of a moderate increase in receiver
2 complexity. Bit error rate reduction has been achieved using
3 trellis CPM demodulation with ideal synchronization. There is a
4 continuing need to develop hardware implementation of the symbol
5 time and carrier phase synchronizers that provides required
6 tracking functions for the coherent CPM receiver. Often, symbol
7 time tracking and carrier phase tracking limit the performance of
8 CPM systems.

9
10 A particular type of CPM system is a Gaussian minimum shift
11 keying (GMSK) system where a data sequence is precoded and the
12 precoded data symbols are used for continuous phase modulation. The
13 GMSK received signals are filtered using Laurent filters and
14 samplers for providing data samples subject to trellis demodulation
15 for generating an estimate of the data sequence. Carrier phase
16 tracking loops are used for demodulating the received signal by
17 tracking the carrier phase, and symbol time tracking loops are used
18 for synchronized sampling of Laurent matched filter signals for
19 generating the data samples that used to generate estimates of the
20 transmitted bit stream using trellis demodulation. These carrier
21 phase and symbol time tracking loops are often referred to as
22 synchronizer. These synchronizers often lose track during noisy
23 communications.

24
25 A binary continuous phase modulation signal can be described
26 by complex envelop equations.

$$z(t) = \operatorname{Re}(z_b(t)e^{j2\pi f_c t})$$

$$z_b(t) = \sqrt{2E_b / T_e} e^{j\phi(t, \alpha)}$$

$$\phi(t, \alpha) = \pi h \int_{-\infty}^t \sum_{n=0}^{N-1} \alpha_n f(t - nT) dt$$

$$= \pi h \sum_{n=0}^{N-1} \alpha_n g(t - nT)$$

The term $z_b(t)$ is called the complex envelope of the CPM signal, f_c is the carrier frequency, E_b is the bit energy, T is the bit duration, and N is the transmitted data length in bits, $\alpha = (\alpha_0 \alpha_1 \dots \alpha_{N-1})$, $\alpha_i \in \{\pm 1\}$, represents one of 2^N equally probable data sequences. The parameter h is the modulation index, $f(t)$ is the pulse response of the smoothing filter in the CPM modulator, and $g(t)$ is the CPM phase response defined in terms of the $f(t)$ pulse response.

$$g(t) = \int_{-\infty}^t f(s) ds$$

The pulse response $f(t)$ is limited to the time interval $[0, LT]$ for some integer L and having the properties that $f(t) = f(LT - t)$ and $g(LT) = 1$. The pulse amplitude modulation (PAM) representation of signal CPM envelope is well known. Laurent has shown that the complex envelope $z_b(t)$ can be expressed as a double summation.

$$z_b(t) = \sqrt{2E_b / T} \sum_{k=0}^{2^{L-1}-1} \sum_{n=0}^{N-1} a_{k,n} h_k(t - kT)$$

In this PAM representation of the baseband CPM signal envelope, also referred to as the Laurent decomposition, the $a_{k,n}$ values are known as pseudo data symbols and are related to the modulated data symbols generally by a pseudo data symbol equation.

$$a_{k,n} = \exp(jh\pi[\sum_{m=0}^n \alpha_m - \sum_{i=0}^{L-1} \alpha_{n-i} \beta_{k,i}])$$

In the pseudo data symbol equation, for all k , $0 \leq k \leq 2^{L-1}$, $\beta_{k,0}=0$ and β_{ki} is a 0 or 1 digit in the binary expansion of $k = \sum_{i=1}^{L-1} 2^{i-1} \beta_{k,i}$. These pseudo data symbols take on values in the set $\{\pm 1, \pm j\}$ when the modulation index h equals $1/2$. In general, the first two pseudo data symbols, $a_{0,n}$ and $a_{1,n}$ can be written in an expanded form.

$$a_{0,n} = \exp(j\pi h \sum_{m=0}^n \alpha_m) = a_{0,n-1} J^{\alpha_n}, \quad a_{0,-1} = 1, \quad J = e^{j\pi h}$$

$$a_{1,n} = a_{0,n-L} J^{\alpha_n} J^{\alpha_{n-2}} J^{\alpha_{n-3}} \dots J^{\alpha_{n-L+1}}$$

The set of pulse functions $\{h_k(t)\}$, termed Laurent pulse functions, have a real value and are finite in duration, and are formed by an $h_k(t)$ equation.

$$h_k(t) = \prod_{i=0}^{L-1} c(t + iT + (\beta_{k,i} - 1)LT)$$

where

$$c(t) = \begin{cases} \sin(\pi h - \pi h g(|t|)) / \sin(\pi h), & |t| \leq LT \\ 0, & \text{elsewhere} \end{cases}$$

Among these $h_k(t)$ pulses, most of the signal energy is carried by the principal Laurent pulse $h_0(t)$, which has a duration of $L+1$ bit times. Another property of the principal Laurent pulse $h_0(t)$ is that it is symmetrical about $t=(L+1)T/2$. The principal Laurent function $h_0(t)$ output provides a gross estimate of the transmitted symbol sequence. These properties of the principal Laurent pulse function $h_0(t)$ have not yet been exploited in developing the error signals for the symbol time and carrier phase tracking loops. These and other disadvantages are solved or reduced using the invention.

1
2 Summary of the Invention
3

4 An object of the invention is to provide data aided symbol
5 timing tracking in continuous phase modulation communication
6 systems.
7

8 Another object of the invention is to provide data aided
9 symbol timing tracking in a Gaussian minimum shift keying
10 communications systems.
11

12 Yet another object of the invention is to provide data aided
13 carrier phase tracking in continuous phase modulation communication
14 systems.
15

16 Still another object of the invention is to provide data aided
17 carrier phase tracking in a Gaussian minimum shift keying
18 communications systems.
19

20 Still another object of the invention is to provide data aided
21 carrier phase synchronizers and symbol time synchronizers in
22 Gaussian minimum shift keying communications systems using
23 principal Laurent responses for generating carrier phase and symbol
24 time errors.
25
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27

28 ///

1 The present invention is directed to data aided
2 synchronization in digital carrier phase and symbol timing
3 synchronizers applicable to precoded continuous phase modulation
4 (CPM) signal formats, such as in Gaussian minimum shift keying
5 (GMSK) communications systems having, for example, a modulation
6 index of $1/2$ with a bandwidth time product (BT) of $1/5$. The
7 imbedded synchronizers enable simple implementations for data
8 demodulation for CPM signals, such as GMSK signals with small BT
9 values. Data aided tracking is applied in one form to symbol time
10 tracking, and in another form, to carrier phase tracking. An
11 advantage of the proposed data aided symbol timing synchronizer is
12 the combination of both symbol timing tracking and data
13 demodulation functions into an integrated process obviating the
14 need for a separate data demodulator in the receiver. For example,
15 for GMSK signals with BT values of $1/3$ and larger, the data
16 demodulation performance in the symbol timing synchronizer can
17 provide optimum performance. An advantage of the data aided carrier
18 phase synchronizer is the combination of both carrier phase
19 tracking and data demodulation functions into one integrated
20 process obviating a need for separate data demodulator in the
21 receiver. For example, for GMSK signals with BT values of $1/3$ and
22 larger, the data demodulation performance provided by the carrier
23 phase synchronizer can also be optimum.

24
25 In the first form, the symbol time tracking synchronizer
26 includes a data aided symbol timing error discriminator that
27 extracts the timing error of the received CPM signal from the
28 principal Laurent amplitude modulation component by an early and

1 late gating operation followed by a multiplication of the data
2 decision to remove the data modulation in the error signal. This
3 symbol timing error signal is then tracked by a second order
4 digital loop operating at the symbol rate. In the second form, the
5 carrier phase tracking synchronizer includes a data aided phase
6 error discriminator that extracts the phase error of the received
7 CPM signal from the principal Laurent amplitude modulation
8 component by a cross correlation operation with the data decision
9 produced by a serial data demodulator. This error signal is then
10 tracked by a second order digital loop also operating at the symbol
11 rate.

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These digital synchronizers are used to track the symbol timing or carrier phase of a continuous phase modulation signal received in the presence of noise with the receiver operating in a data demodulation mode. These synchronizers have a nondegraded bit error rate (BER) performance with reduced design complexity. The GMSK signal with a $BT=1/5$ can be used as a typical partial response CPM signal. The hardware implementation of such a GMSK receiver with both synchronizers can be modeled for providing simulated BER performance. With data precoding of the original data bit stream prior to transmission of the CPM signal, the synchronizers can function as serial demodulators that achieve absolute phase data detection. The data precoding and data aided synchronization approach for detecting symbol timing and carrier phase error is central to providing accurate symbol time and carrier phase tracking in the synchronizers with reduced design complexity. These and other advantages will become more apparent from the following detailed description of the preferred embodiment.

///

Brief Description of the Drawings

Figure 1A is a block diagram of a symbol time synchronized data demodulator.

Figure 1B is a block diagram of a symbol time synchronizer.

Figure 2A is a block diagram of a carrier phase synchronized data demodulator.

Figure 2B is a block diagram of a carrier phase synchronizer.

Figure 3 is a graph depicting Laurent pulse functions.

Figure 4 is a graph depicting an early-late gate function.

Figure 5 is a plot of a symbol time error discriminator curve.

Figure 6 is a plot of a carrier phase discriminator curve.

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Detailed Description of the Preferred Embodiment

An embodiment of the invention is described with reference to the figures using reference designations as shown in the figures. Referring to Figure 1A, a symbol time synchronized data demodulator includes a symbol time synchronizer 10 for data demodulating an $r(t)$ received signal 11 sampled by input sampler 12 using a generated t_n timing signal 13. The $r(t)$ received signal 11 is a combination of the transmitted signal $z_b(t)$ and noise $n(t)$ and is converted into an r_n sampled input signal 14. The synchronizer 10 receives the sampled input signal 14 and provides a \hat{d}_n estimate 15 of the received data sequence of the r_n sampled input 14 as well as generating a t_{mN} timing signal 17 and t_n timing signal 13. The r_n sampled input 14 can be communicated to conventional Laurent matched filters such as a principal Laurent matched filter 18 and a secondary Laurent matched filter 19 having respective principal and secondary matched filter outputs respectively sampled by samplers 20 and 21 for providing respective filter samples into a Viterbi algorithm demodulator 22 that provides a \hat{d}_m estimate 23. The matched filters 18 and 19, samplers 20 and 21, and demodulator 22 are used to generate the \hat{d}_m estimate 23 of the original data sequence using the symbol timing of the t_{mN} 17 timing signal generated by the symbol time synchronizer 10. The filters 18, 19 samplers 20 and 21, and demodulator 22 providing the \hat{d}_m data estimate 23 represents conventional data demodulation.

///

1 Referring to Figures 1A and 1B, and more particularly to the
2 symbol time synchronizer of Figure 1B, a real component and an
3 imaginary component of the r_n sampled input signal 14 are
4 respectively isolated by an inphase component isolator 24 and a
5 quadrature component isolator 26 respectively providing inphase and
6 quadrature sample signals to an odd timing error detector 32 and an
7 even timing error detector 34, that in turn, provide respective odd
8 data and even data signals to a data demultiplexer 36 that provides
9 the \hat{d}_n estimated data sequence 15. The odd timing error detector 32
10 and even timing error detector 34 receive the inphase and
11 quadrature sampled signals that are respectively communicated to
12 early-late gates 44a and 44b and Laurent transformers $h_D(t)$ 46a and
13 46b isolating principal Laurent components. The Laurent transformer
14 outputs of the transformers 46a and 46b are sampled by samplers 47a
15 and 47b providing transformed sampled outputs. The early-late gate
16 outputs of the early-late gates 44a and 44b are sampled by gate
17 samplers 48a and 48b providing gate sampled outputs, respectively.
18 The transformer sampled outputs of the transformer samplers 47a and
19 47b are respectively communicated to hard limiters 50a and 50b. The
20 gate sampled outputs of the gate samplers 48a and 48b are
21 respectively communicated to mixers 52a and 52b. The hard limiters
22 52a and 52b respectively provide the odd data and even data to the
23 data demultiplexer 36 that provides the \hat{d}_n estimated data 15. The
24 mixers 52a and 52b respectively mix odd and even data with the gate
25 sampled outputs of gate samplers 48a and 48b to respectively
26 provide e_{2k+1} odd and e_{2k} even timing signals that drive a loop
27 filter 53, that in turn, controls a voltage controlled oscillator
28 54 used for generating the t_n timing signal. The t_n timing signal 13

1 is further communicated to a modulo N counter 55 that provides the
2 t_{mN} timing signals as well as generating the e_{2k+1} odd and e_{2k} even
3 sampling signals that respectively control the samplers 47a and
4 47b, and, 48a and 48b. As may now be apparent, the synchronizer 10
5 operates in a timing loop extending through samplers 47ab, limiters
6 50ab, mixers 52ab, loop filter 53, VCO 54 and counter 55 for
7 synchronized generation of the odd and even data and the t_n and t_{mN}
8 timing signals, 13 and 17, respectively, while generating the \hat{d}_n
9 data estimates 15.

10
11 Referring to Figures 1A, 1B, 2A and 2B, and more particularly
12 to Figures 2A and 2B, the carrier phase synchronizer demodulator of
13 Figure 2A and specifically the carrier phase synchronizer 60 of
14 Figure 2B, the carrier phase synchronizer 60 generates a $e^{-j\hat{\theta}}$ phase
15 adjustment signal 59 for adjusting the phase of the $r(t)$ input
16 signal 11. The carrier phase synchronizer 60 also receives an $r_n e^{-j\hat{\theta}}$
17 input sample signal 61 from a carrier phase sampler 62. The $r(t)$
18 received input signal 11 and $e^{-j\hat{\theta}}$ phase adjustment signal are mixed
19 by a mixer 63 that provide an input mixed signal that is sampled by
20 a carrier phase sampler 62 at the rate of the t_n timing signal for
21 providing the $r_n e^{-j\hat{\theta}}$ sampled input signal 61 to the carrier phase
22 synchronizer 60. The $r_n e^{-j\hat{\theta}}$ input sampled signal 61 can be fed into
23 a conventional principal Laurent matched filter 64 and a secondary
24 Laurent filter 66 providing matched filters outputs respectively to
25 and sampled by matched filtered samplers 68 and 70 sampled at the
26 rate of the t_{mN} symbol timing signals for providing matched filter
27 inputs into a Viterbi algorithm demodulator 72 that generates a \hat{d}_m
28 estimate 73 of the original data sequence. The carrier phase

1 synchronizer 60 can also be used to generate the \hat{d}_n data estimate
2 15.

3
4 The carrier phase synchronizer 60 receives the t_n timing signal
5 that may originate from the symbol time synchronizer 10 in the
6 preferred form, or from a convention symbol timing tracking loop,
7 not shown. The $r_n e^{-j\hat{\theta}}$ sample input signal 61 is communicated to an
8 inphase component isolator 74 and a quadrature component isolator
9 76. The inphase component output of isolator 74 and the quadrature
10 component output of isolator 76 are respectively sampled by an
11 inphase sampler 80 and a quadrature sampler 82 at the rate of the t_n
12 symbol timing signal 13 that also drives a modulo N counter 84
13 providing $2kN$ even and $(2k+1)N$ odd timing sampling signals. The
14 inphase sampler 80 provides a sampled inphase signal to an inphase
15 transformer 86 as the quadrature sampler 82 provide a sampled
16 quadrature signal to a quadrature transformer 88, providing
17 respectively inphase and quadrature transformed signals to hard
18 limiters 90a and 90b, and by cross coupling, to mixers 92b and 92a.
19 The hard limiters 90a and 90b respectively provide inphase and
20 quadrature hard limited signals to hard limiter samplers 94a and
21 94b that respectively sample at rates of the $2kN$ even and $(2k+1)N$
22 odd timing sampling signals from the modulo N counter 84. The hard
23 limiter samplers 94a and 94b respectively provide odd and even data
24 signals that are fed into a data demultiplexer 94 for generating
25 the \hat{d}_n data estimate 15. The odd data and even data are respectively
26 mixed with the quadrature and inphase transformed signals from the
27 transformers 88 and 86, respectively, by the mixer 92a and 92b, for
28 generating e_{2k+1} odd and $-e_{2k}$ even timing error signals. The $-e_{2k}$

1 timing error signal is inverted by inverter 96 for generating an e_{2k}
2 even timing signal. The e_{2k} even and e_{2k+1} odd timing error signals
3 drive a loop filter 97 that in turn controls a VCO 98 that
4 generates the $e^{-j\hat{\theta}}$ phase adjustment signal 59. As may now be
5 apparent, the carrier phase synchronizer 60 is part of a loop
6 between the $e^{-j\hat{\theta}}$ phase adjustment signal 59 and the $r_n e^{-j\hat{\theta}}$ input
7 sampled signal 61 with the loop extending through the isolators 74
8 and 76, samplers 80 and 82, transformers 86 and 88, hard limiters
9 90a and 90b, samplers 94a and 94b, mixers 92a and 92b, loop filter
10 97 and VCO 98 for providing the $e^{-j\hat{\theta}}$ phase adjustment signal 59,
11 while concurrently generating the \hat{d}_n data estimate 15.

12
13 Referring to all of the Figures, the Laurent pulse function is
14 shown in Figure 3 for the principal h_0 pulse function, the $h_1(t)$
15 secondary pulse function and the $h_2(t)$ tertiary pulse function. The
16 inphase component isolators 24 and 74 isolate the real component of
17 the r_n input signal as the quadrature component isolators 16 and 76
18 isolate the imaginary component of the r_n input signal. The inphase
19 Laurent transformers 46a and 86 isolate the energy of the principal
20 Laurent pulse component of the real component of the r_n input signal
21 as the quadrature Laurent transformers 46b and 88 isolate the
22 energy of the principal Laurent pulse component of the imaginary
23 component of the r_n input signal. The early-late gate function is
24 shown in Figure 4 for providing a digital transition in synchronism
25 with Laurent components as isolated by the isolators 24 and 26. In
26 the symbol timing synchronizer 10, the early-gates 44a and 44b
27 operate on the respective isolated real and imaginary component
28 energy for indicating the magnitude of the symbol timing error. The

1 early-late gates 44a and 44b ideally have a positive value and a
2 negative value on early and late respective sides of the center of
3 the principal Laurent pulse function. These +/- values are combined
4 with respective sides of the principal Laurent pulse function to
5 provide two equal but opposite products that ideally sum to a zero
6 magnitude error. As the principal Laurent pulse function early or
7 late shifts relative to the current timing of the +/- gate
8 function, the magnitude error increases positively or negatively.
9 The area under the principal Laurent pulse function is multiplied
10 by the gate function to produce a cross correlation of the gate
11 function and principal Laurent pulse function for generating the
12 magnitude error value that is used to adjust the timing signal to
13 be in synchronism with the current symbol time of the received
14 signal. Figure 5 shows symbol timing errors for the symbol timing
15 synchronizer 10.

16
17 The carrier phase synchronizer 60 uses the Laurent
18 transformers 86 and 88 for isolating the energy of the principal
19 Laurent pulse component for generating the magnitude of the carrier
20 phase error. The carrier phase synchronizer 60 also uses cross
21 coupled principal Laurent pulse energy for indicating the sign of
22 the carrier phase error. Figure 6 shows the carrier phase errors of
23 the carrier phase synchronizer 60.

24
25 The symbol time synchronized data demodulator includes the
26 symbol time synchronizer 10 for generating the t_n timing signal 13
27 as well as the \hat{d}_n data estimates 15. The carrier phase synchronizer
28 60 receives the t_n symbol timing signal 13 for sampling the real and

1 imaginary isolated components as well as for generating the odd and
2 even data of the \hat{d}_n data estimates 15. Hence, both of the
3 synchronizers 10 and 60 operate as serial data demodulators for
4 generating the \hat{d}_n data estimate 15. Both of the symbol timing and
5 carrier phase serial demodulators of synchronizers 10 and 60
6 operate respective modulo N counters 55 and 84 at the rate of N
7 counts per symbol period of T seconds clocked at the rate of the t_n
8 symbol timing signal 13. The complex envelope $z_p(t)$ of the CPM input
9 signal 11 is sampled at a uniform rate of N samples per symbol
10 period. These r_n samples are simultaneously applied to the Laurent
11 transformers 46a, 46b, 86, and 88 that function as data detection
12 filters.

13 In the symbol timing synchronizer 10, the early-late gates 44a
14 and 44b function as impulse response filters. At each symbol
15 decision instant of $t=KN$ sample counts, for odd values of K, i.e.,
16 $K=2k+1$, the timing error between the receiver t_n timing signal 13
17 and the timing of the received signal is formed by respectively
18 multiplying the output of the early-late gate 44a the algebraic
19 sign of the respective data detection filter, that is, the
20 transformer 46a and hard limiters 50a. For even values of K, i.e.,
21 $K=2k$, the even timing error detector 34 operates similar to the odd
22 time error detector 32. The algebraic sign of the data detection
23 filter outputs, that is, the output of the hard limiters 50a and
24 50b, is a data decision on the received data symbol for precoded
25 binary CPM received signals. The timing error formed by the
26 detectors 32 and 34 is then filtered by the loop filter 53,
27 integrated by the VCO 54, and quantized into sample counts by the
28 modulo N counter 55 to produce an adjustment to the sampling timing

1 at symbol epoch i.e., at time instants of a multiple of N counts.
2 The symbol timing signal 13 as well as the sampling signals are
3 delayed or advanced by the timing adjustment according to whether
4 the adjustment is positive or negative. No more than N most recent
5 signal samples need to be stored by the synchronizer to allow for
6 the advancing of the sampling timing at the symbol time in the
7 tracking mode.

8
9 During data demodulation, the transmitted data symbol can be
10 obtained by differentially decoding two successively received
11 pseudo data symbols $a_{0,n}$. For a CPM modulation index of $h=0.5$, the
12 data stream is precoded into a data stream d_k fed into the data
13 modulator having an input symbol stream α_k with $\alpha_k = (-1)^k d_{k-1} d_k$. The
14 pseudo data symbol $a_{0,n}$ becomes $a_{0,n} = J(n) d_n$ with $J(n)=1$ for n being
15 odd and $J(n)=j$ for n being even. Thus, with data precoding, either
16 a conventional trellis demodulator or a serial demodulator of the
17 synchronizers 10 and 60 can be used to demodulate the received CPM
18 signal without differential decoding. A CPM modem using precoding
19 can achieve a performance improvement from 0.5dB to nearly 2.0dB
20 over a modem without precoding.

21
22 Because the Laurent pulse function $h_0(t)$ is the dominant pulse
23 function in a CPM signal, the symbol timing error of the received
24 signal relative to the receiver clock can be detected by using the
25 early-late gating on the received baseband signal in conjunction
26 with serial data demodulation of the synchronizers 10 and 60. The
27 timing error is produced by respectively multiplying the data
28 decisions generated by the serial demodulation of the transformers

1 46a and 46b and the hard limiters 50a and 50b with the output of
 2 the early-late gate 44a and 44b. Respective multiplication by
 3 mixers 52a and 52b of the early-late gate output with hard limited
 4 data decisions is needed to eliminate the data modulation so that a
 5 consistent timing error can be formed. With ideal elimination of
 6 the data modulation, the detected timing error is given by a
 7 detection equation.

$$D_t(\tau) = \int_0^{(L+1)T} G(s)h_0(s - \tau)ds$$

14 The early-late gate function $G(t)$ provides an ideal timing
 15 error detection curve $D_t(\tau)$ for a given CPM signal, such as a $BT=1/5$
 16 GMSK signal.

18 Carrier phase error detection is formulated based on a unit
 19 amplitude CPM signal received in the absence of channel noise with
 20 a carrier phase offset θ . The phase offset complex signal envelope
 21 is defined by an $r(t, \theta)$ equation.

$$\begin{aligned} r(t, \theta) &= z_b(t)e^{j\theta} \\ &= \left\{ \sum_{k=0}^{Q-1} \sum_{n=0}^{N-1} a_{k,n} h_k(t - nT) \right\} e^{j\theta} \end{aligned}$$

When the $r(t, \theta)$ signal is applied to the transformed and hard limited serial demodulator, the demodulator output at time $t=mT$ is defined by an r_m equation.

$$\begin{aligned} r_m &= \int_{-\infty}^{\infty} r(t, \theta) h_0(t - mT) dt \\ &= \left\{ \sum_{k=0}^{Q-1} \sum_{n=0}^{N-1} a_{k,n} R_{0,k}(m - n) \right\} e^{j\theta} \\ &= J(m) d_m e^{j\theta} R_{0,0}(0) + \left\{ \sum_{k=0}^{Q-1} \sum_{\substack{n=0 \\ (n \neq m, \\ k=0)}}^{N-1} a_{k,n} R_{0,k}(m - n) \right\} e^{j\theta} \end{aligned}$$

where

$$R_{0,k}(p) = \int_{-\infty}^{\infty} h_0(t) h_k(t + pT) dt$$

With the data d_k being equally probable, the averaged value of $d_m a_{k,n}$ is zero for all integers m , when $k \neq 0$, and also for all integers $m \neq n$ when $k=0$. Thus, with the carrier phase error θ being small and when the serial demodulators can correctly demodulate the m -th transmitted bit d_m , then, by multiplying the serial demodulated bit by the complex conjugate of $J(m) d_m$ and taking the imaginary part of the product obtains a random variant whose mean value is $D_\phi(\theta) = R_{0,0}(0) \sin(\theta) \approx R_{0,0}(0) \theta$. The randomness is due to the intersymbol interference, which is data pattern dependent.

Because both timing and carrier phase error detection use serial demodulation to provide the required data decision for error generation, the transformed and hard limited serial demodulator,

such as in the synchronizers 10 and 60, can be used for both the tracking error generation and data detection. The error signals produced at every receiver symbol time are applied to the respective loop filter 53 and 97 and voltage control oscillator 54 and 98 to adjust the sampling timing instants or the carrier phase to the received signal. Data reliability of a trellis demodulator is usually better than that of a serial demodulator such as the synchronizers 10 and 60, particularly when the signal memory span L is large. However, if L is small or if an equalizer is used in cascade with the principal Laurent pulse filter, the simple serial receiver can perform practically as well as the more complex trellis demodulator for the purpose of tracking error generation. Thus, an equivalent variation of the synchronizers 10 and 60 is to feedback the data decisions from the trellis demodulator to the error detectors, provided that the processing delay of the trellis demodulator is properly compensated for and that tracking performance is not unduly compromised by the delay.

The mean error output or discriminator characteristics of the symbol timing error and carrier phase error detectors is shown for the $BT=1/5$ GMSK signal, in Figure 5 and Figure 6, respectively. These characteristics are obtained by computing in random data the averaged detector output for a given error offset with the other offset error set at zero. For small errors, the linear slope of the timing error discriminator curve is about -1.5 and that of the phase error discriminator curve is about 1.0. The deviation of these characteristics from their ideal S curves, at large offset

errors, is attributed to the feedback of erroneous data decisions caused by the intersymbol interference in the GMSK signal.

Both the symbol time synchronizer 10 and carrier phase synchronizer 60 have a linear continuous time model that can be implemented digitally for use in performance simulations of the GMSK receiver. The linear model is appropriate because the tracking error is typically small when the receiver is in a tracking mode. The loop filter, used in each synchronizer 10 and 60, is of a proportional and integral type with a transfer function in the form of $F(s) = \alpha + \beta/s$ and the VCO transfer function in the form of K_v/s where K_v is the VCO gain. The closed loop transfer function of the synchronizers 10 and 60 is defined by an $H(s)$ equation.

$$H(s) = \frac{\phi_o(s)}{\phi_i(s)} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

In the $H(s)$ equation, the term ζ is the damping factor and ω_n is the natural frequency of the synchronizers 10 and 60. These parameters are related to the loop filter and gain parameters by $\alpha = 2\zeta\omega_n/K_D K_v$ and $\beta = \omega_n^2/K_D K_v$ where K_D is the slope of the error discriminator curves shown in Figures 5 and 6. The one-sided equivalent noise bandwidth of the synchronizers 10 and 60 is $B_L = (\omega_n/8\zeta)(1+4\zeta^2)$. Each of the second order synchronizers 10 and 60 can be digitally implemented with the integrator $1/s$ approximated by the digital accumulator $1/(1-z^{-1})$ where z^{-1} represents a unit bit

1 time delay. In a digital implementation, the natural frequency and
2 loop bandwidth parameters should be regarded as parameters
3 normalized by the bit rate. Using the loop parameters $K_D=1$, $K_V=1$ and
4 $\zeta=1/\sqrt{2}$ for the carrier phase synchronizer 60 and $K_D=\sqrt{1.5}$, $K_V=1$ and
5 $\zeta=1/\sqrt{2}$ for the symbol time synchronizer 10, the step error response
6 of the carrier phase synchronizer 60 to a 20 degree phase step and
7 that of the symbol time synchronizer 10 to a half bit time step are
8 simulated and compared to the theoretical step error response. The
9 ramp error responses for both synchronizers 10 and 60 are also
10 simulated and compared to the theoretical ramp error responses. The
11 dispersion of the simulated error responses from the theoretical is
12 due to the intersymbol interference in the received signal.

13
14 The symbol time synchronizer 10 and carrier phase synchronizer
15 60 are characterized as providing error signals generated from
16 quadrature Laurent pulse response components of a receiving signal
17 modulated by symbols generated from a precoded data sequence. In
18 the preferred form, the principal Laurent components indicates the
19 original digital bit sequence of the precoded bit stream. The
20 precoding functions to precondition the transmitted symbol sequence
21 so that the principal Laurent function indicates the original data
22 bit stream that is alternately disposed on the I and Q channels of
23 the transmitted CPM signal.

24
25 The precoded PCM signal allows the use of the principal
26 Laurent pulse response for extracting the sign of the symbol timing
27 error or carrier phase error that is also the data of the original
28 data uncoded sequence. In the symbol time synchronizer 10, the

1 early-late gates 44a and 44b will extract the magnitude of the
2 symbol timing error. The early-late gates 44a and 44b are sampled
3 at the current symbol t_n timing signal 13. As the timing of the
4 received signal 11, varies from the current timing of the timing
5 signal 13, the early-late gates 44a and 44b provide an indication
6 of the magnitude of the current timing error. The CPM signal will
7 carry the data information in one symbol time in the inphase
8 component signal and in the next symbol instance in the quadrature
9 component signal, as the data bit information content alternates
10 between the inphase and quadrature components. The timing
11 synchronizer 10 in combination with data precoding enable efficient
12 synchronization timing and data extraction at the expense of
13 requiring the use of both I & Q component signals that might
14 otherwise be used to communicate two independent data streams. The
15 loop filter 53 functions to smooth the timing error signal
16 generated by the detectors 32 and 34. The smoothed timing error
17 from the loop filter 53 then drives the VCO that in turn provides
18 the smoothly varying t_n timing clock signal. The precoded data
19 provides the sign of the timing error, and hence, the symbol timing
20 synchronizer 10 is data aided, and hence also provides an estimate
21 of the original data sequence.

22
23 In the carrier phase synchronizer receives the t_n timing signal
24 and the received signal r_n and operates on the phase error θ
25 generated from the $r(t, \theta)$ equation that describes the phase error.
26 The carrier phase synchronizer 60 also uses the isolated I & Q
27 principal Laurent components and determines the sign of the phase
28 error. But, rather than determining a magnitude of the phase error

1 using early-late gates, the carrier phase synchronizer drifts the
2 phase error depending on the sine of the phase error having a sign
3 that is also the original uncoded data sequence. The $\hat{\theta}$ term
4 represents the carrier phase error that is generated using cross-
5 coupling of the Laurent components generating the e_{2k} and e_{2k+1}
6 error signals with the sign of $\hat{\theta}$ indicating the direction of the
7 phase error drift.

8
9 The symbol timing synchronizer 10 and the carrier phase
10 synchronizer 60 offer an efficient mechanism for generating timing
11 and phase error signal while also providing an indication of the
12 uncoded data sequence however requiring data precoding having
13 symbol modulated on both I and Q channels. Those skilled in the art
14 can make enhancements, improvements, and modifications to the
15 invention, and these enhancements, improvements, and modifications
16 may nonetheless fall within the spirit and scope of the following
17 claims.

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2 What is claimed is:

3
4 1. A symbol timing synchronizer for generating a timing signal from
5 a sampled input signal being a received input signal sampled at a
6 rate of the timing signal, the received input signal being a
7 continuous phase modulated signal modulated by a symbol sequence
8 generated from a precoded data sequence of an input data sequence,
9 sampled input signal having a sampled inphase component and a
10 sampled quadrature component, the symbol timing synchronizer
11 comprising,

12 an inphase isolator and a quadrature isolator for respectively
13 isolating the sampled inphase component and sampled quadrature
14 component of the sampled input signal for respectively providing an
15 inphase signal and a quadrature signal,

16 an inphase serial data demodulator and a quadrature serial
17 data demodulator for respectively receiving and filtering the
18 inphase signal and the quadrature signal for generating an odd
19 filter response and an even filter response, and for converting and
20 sampling the odd and even filter responses into odd data and even
21 data, the odd data and the even data alternately forming an
22 estimate of the input data sequence,

23 an inphase error magnitude generator and a quadrature error
24 magnitude generator for receiving and filtering the inphase signal
25 and the quadrature signal, for respectively generating and sampling
26 an inphase error magnitude signal and quadrature error magnitude
27 signal for respectively generating a sampled inphase error
28 magnitude signal and a sampled quadrature error magnitude signal,

an inphase mixer and a quadrature mixer for respectively mixing the sampled inphase error magnitude signal with the odd data into an odd error signal, and mixing the quadrature error magnitude signal with the even data for generating an even error signal, the odd data representing an odd sign of the inphase magnitude error signal, the even data representing an even sign of the quadrature magnitude signal, and

an oscillator means for generating the timing signal from the even error signal and the odd error signal, the timing signal for controlling the sampling of the inphase serial data demodulator and the quadrature serial data demodulator and for controlling the sampling of inphase error magnitude generator and a quadrature error magnitude generator for generating the timing signal at a rate of the symbol sequence.

2. The symbol timing synchronizer of claim 1 wherein the oscillator means comprises,

a loop filter for receiving the odd error signal and the even error signal for providing a filter error signal,

a controlled oscillator for receiving the filter error signal for generating the timing signal, and

a modulo counter for providing an odd timing signal for sampling the inphase magnitude error signal, and for providing an even timing signal for sampling the quadrature magnitude error signal.

1 3. The symbol timing synchronizer of claim 1 wherein,
2 the inphase magnitude error generator generates the inphase
3 magnitude error signal from a difference between a filter response
4 of the inphase signal and an odd modulo count of the timing signal,
5 the inphase magnitude error generator serving to cross correlate a
6 principal Laurent component of the inphase signal with a gate
7 function relative to the odd modulo count of the timing signal, and
8 the quadrature magnitude error generator generates the
9 quadrature magnitude error signal from a difference between a
10 filter response of the quadrature signal and an even modulo count
11 of the timing signal, the quadrature magnitude error generator
12 serving to cross correlate a principal Laurent component of the
13 inphase signal with a gate function relative to the even modulo
14 count of the timing signal.

15
16
17 4. The symbol timing synchronizer for claim 1 wherein,
18 inphase and quadrature serial demodulators respectively filter
19 principal Laurent components of the inphase and quadrature signals
20 for providing odd and even Laurent filter responses, and
21 inphase and quadrature serial demodulators respectively
22 sample the odd and even Laurent filter responses for generating the
23 odd and even data.

24
25
26 5. The symbol timing synchronizer of claim 1 further comprising
27 an input sampler for sampling the received signal into the
28 sampled input signal sampled at a rate of the timing signal.

1 6. The symbol timing synchronizer of the claim 1 further
2 comprising,

3 a multiplexer for multiplexing the odd and even data into the
4 estimate of the input data sequence.

5
6 7. the symbol timing synchronizer of claim 1 wherein,

7 the received input system is a Gaussian minimum shift keying
8 signal have a bit bandwidth product of $1/5$ and a modulation index
9 of $1/2$.

10
11 8. The symbol timing synchronizer of claim 3 wherein,

12 the odd modulo count is $(2k+1)N$ where N is the modulo count of
13 the modulo counter, and

14 the even modulo count is $(2k)N$ where N is the modulo count of
15 the modulo counter

16
17 9. The symbol timing synchronizer of claim 1 wherein

18 the odd error signal is an e_{2k+1} odd error signal, and

19 the even error signal is an e_{2k} even error signal.

20
21 10. The symbol timing synchronizer of claim 1 further comprising
22 a carrier phase synchronizer for generating a phase adjustment
23 signal from a sampled phase adjusted input signal and the timing
24 signal,

25 an input mixer for adjusting the received input signal into a
26 phase adjusted input signal, and

27 an input sampler for sampling the phase adjusted input signal
28 into the sampled phase adjusted input signal.

1 11. The symbol timing synchronizer of claim 10 wherein the carrier
2 phase synchronizer comprises,
3 an inphase isolator and a quadrature isolator for respectively
4 isolating the sampled inphase component and sampled quadrature
5 component for providing an inphase signal and a quadrature signal,
6 an inphase serial data demodulator and a quadrature serial
7 data demodulator for respectively receiving and filtering the
8 inphase signal and the quadrature signal for generating an odd
9 filter response and an even filter response, and for converting and
10 sampling the odd and even filter responses into odd data and even
11 data, the odd data and the even data alternately forming an
12 estimate of the input data sequence,
13 an odd mixer and an even mixer for respectively mixing the
14 even filter response and the odd data signal into an odd error
15 signal and mixing the odd filter response signal and the even data
16 signal into an even error signal, and
17 an oscillator means for converting the odd and even error
18 signals into the phase adjustment signal.
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3 12. A symbol timing synchronizer for generating a timing signal
4 from a sampled input signal being a received input signal sampled
5 at a rate of the timing signal, the received input signal being a
6 continuous phase modulated signal modulated by a symbol sequence
7 generated from a precoded data sequence of an input data sequence,
8 sampled input signal having a sampled inphase component and a
9 sampled quadrature component, the symbol timing synchronizer
10 comprising,
11 an inphase isolator and a quadrature isolator for respectively
12 isolating the sampled inphase component and sampled quadrature
13 component of the sampled input signal for respectively providing an
14 inphase signal and a quadrature signal,
15 an inphase early-late gate and a quadrature early-late gate
16 for respectively filtering the inphase signal and the quadrature
17 signal for generating an inphase gate signal and a quadrature gate
18 signal, the inphase and quadrature early-late gates respectively
19 serving to cross correlate the inphase and quadrature signals with
20 gate functions in synchronism with the timing signal,
21 an inphase transformer and a quadrature transformer for
22 respectively transforming the inphase signal and the quadrature
23 signal for generating an inphase transformed signal and a
24 quadrature transformed signal,
25 an inphase gate sampler and a quadrature gate sampler for
26 respectively sampling inphase gate signal and the quadrature gate
27 signal for generating a sampled inphase gate signal and a sampled
28 quadrature gate signal,

1 an inphase transformer sampler and a quadrature transformer
2 sampler for respectively sampling the inphase transformed signal
3 and the quadrature transformed signal for generating a sampled
4 inphase transformed signal and a sampled quadrature transformed
5 signal,
6 an inphase hard limiter and a quadrature hard limiter for
7 respectively converting the sampled inphase transformed signal into
8 odd data and the sampled quadrature transformed signal into even
9 data,
10 an inphase mixer and a quadrature mixer for respectively
11 mixing the sampled inphase gate signal and odd data into an odd
12 error signal and mixing the sampled quadrature gate signal and even
13 data signal into an even error signal, and
14 an oscillator means for generating the timing signal from the
15 even error signal and the odd error signal, the oscillator means
16 for controlling the sampling of the inphase and quadrature gate
17 samplers and the inphase and quadrature transformer samplers for
18 generating the timing signal at a rate of the symbol sequence.

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1 13. The symbol timing synchronizer of claim 12 wherein the
2 oscillator means comprises,

3 a loop filter for receiving the odd error signal and the even
4 error signal for providing a filter error signal,

5 a controlled oscillator for receiving the filter error signal
6 for generating the timing signal, and

7 a modulo counter for providing an odd timing signal for
8 sampling the inphase magnitude error signal, and for providing an
9 even timing signal for sampling the quadrature magnitude error
10 signal.

11
12
13 14. The symbol timing synchronizer of claim 12 wherein,

14 the inphase and quadrature early-late gates function as cross
15 correlators for cross correlating a filter response isolating
16 principal Laurent components of the inphase and quadrature signals
17 with a gating function,

18 the inphase gate signal is an inphase magnitude error signal
19 from the correlation of an inphase early-late gate filter response
20 of the inphase signal and the gating function that is in
21 synchronism with an odd modulo count of the timing signal, and

22 the quadrature gate signal is a quadrature magnitude error
23 signal from the correlation of a quadrature early-late gate filter
24 response of the quadrature signal and the gating function that is
25 in synchronism an even modulo count of the timing signal.

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1 15. The symbol timing synchronizer for claim 12 wherein,
2 the inphase and quadrature transformers, transformer samplers
3 and hard-limiters respectively are inphase and quadrature serial
4 demodulators,

5 the inphase and quadrature transformer are principal Laurent
6 component filters providing the inphase and quadrature transformed
7 signals that respectively are odd and even Laurent filter
8 responses, and

9 the odd and even data alternately forming an estimate of the
10 input data sequence.

11
12 16. The symbol timing synchronizer of claim 12 further comprising
13 an input sampler for sampling the received signal into the
14 sampled input signal sampled at a rate of the timing signal, and
15 a multiplexer for multiplexing the odd and even data into the
16 estimate of the input data sequence.

17
18
19 17. The symbol timing synchronizer of claim 12 wherein,
20 the received input system is a Gaussian minimum shift keying
21 signal have a bit bandwidth product of $1/5$ and a modulation index
22 of $1/2$,

23 the odd modulo count is $(2k+1)N$ where N is the modulo count of
24 the modulo counter,

25 the even modulo count is $(2k)N$ where N is the modulo count of
26 the modulo counter,

27 the odd error signal is an e_{2k+1} odd error signal, and

28 the even error signal is an e_{2k} even error signal.

1 18. The symbol timing synchronizer of claim 12 further comprising
2 a carrier phase synchronizer for generating a phase adjustment
3 signal from a sampled phase adjusted input signal and the timing
4 signal,

5 an input mixer for adjusting the received input signal into a
6 phase adjusted input signal, and

7 an input sampler for sampling the phase adjusted input signal
8 into the sampled phase adjusted input signal.

9
10 19. The symbol timing synchronizer of claim 18 wherein the carrier
11 phase synchronizer comprises,

12 a carrier inphase isolator and a carrier quadrature isolator
13 for respectively isolating the carrier sampled inphase component
14 and carrier sampled quadrature component for providing a carrier
15 inphase signal and a carrier quadrature signal,

16 an inphase sampler and a quadrature sampler for respectively
17 sampling at the rate of the timing signal the carrier inphase
18 signal and the carrier quadrature signal for providing a carrier
19 sampled inphase signal and a carrier sampled quadrature signal,

20 a carrier inphase transformer and a carrier quadrature
21 transformer for respectively transforming the carrier sampled
22 inphase signal and carrier sampled quadrature signal into a carrier
23 inphase transformed signal and a carrier quadrature transformed
24 signal,

25 a carrier inphase hard limiter and a carrier quadrature hard
26 limiter for respectively converting the carrier inphase transformed
27 signal and carrier quadrature transformed signal into a carrier odd
28 hard limited signal and a carrier even hard limited signal,

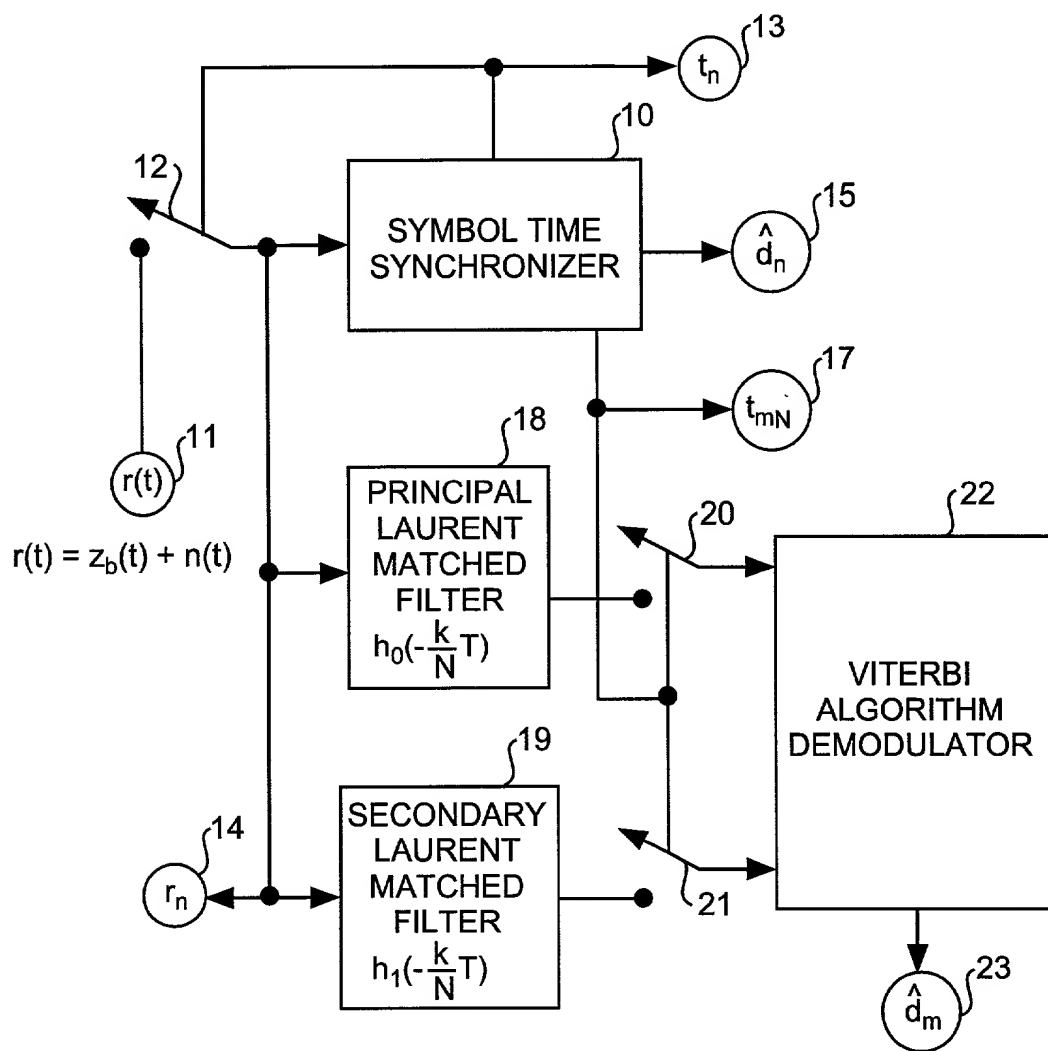
1 a carrier modulo counter for receiving the timing signal and
2 generating a carrier odd timing signal and a carrier even timing
3 signal,
4 a carrier odd sampler and a carrier even sampler for
5 respectively sampling at the rate of the carrier odd and even
6 timing signals for sampling the carrier odd and even hard limited
7 signals into carrier odd data and carrier even data,
8 a carrier odd mixer and a carrier even mixer for respecting
9 mixing the carrier quadrature transformed signal and the carrier
10 odd data signal into a carrier odd error signal and the carrier
11 inphase transformed signal and the carrier even data signal into a
12 carrier even error signal, and
13 a carrier oscillator for converting the carrier odd and even
14 error signals into the phase adjustment signal.

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Abstract of the Disclosure

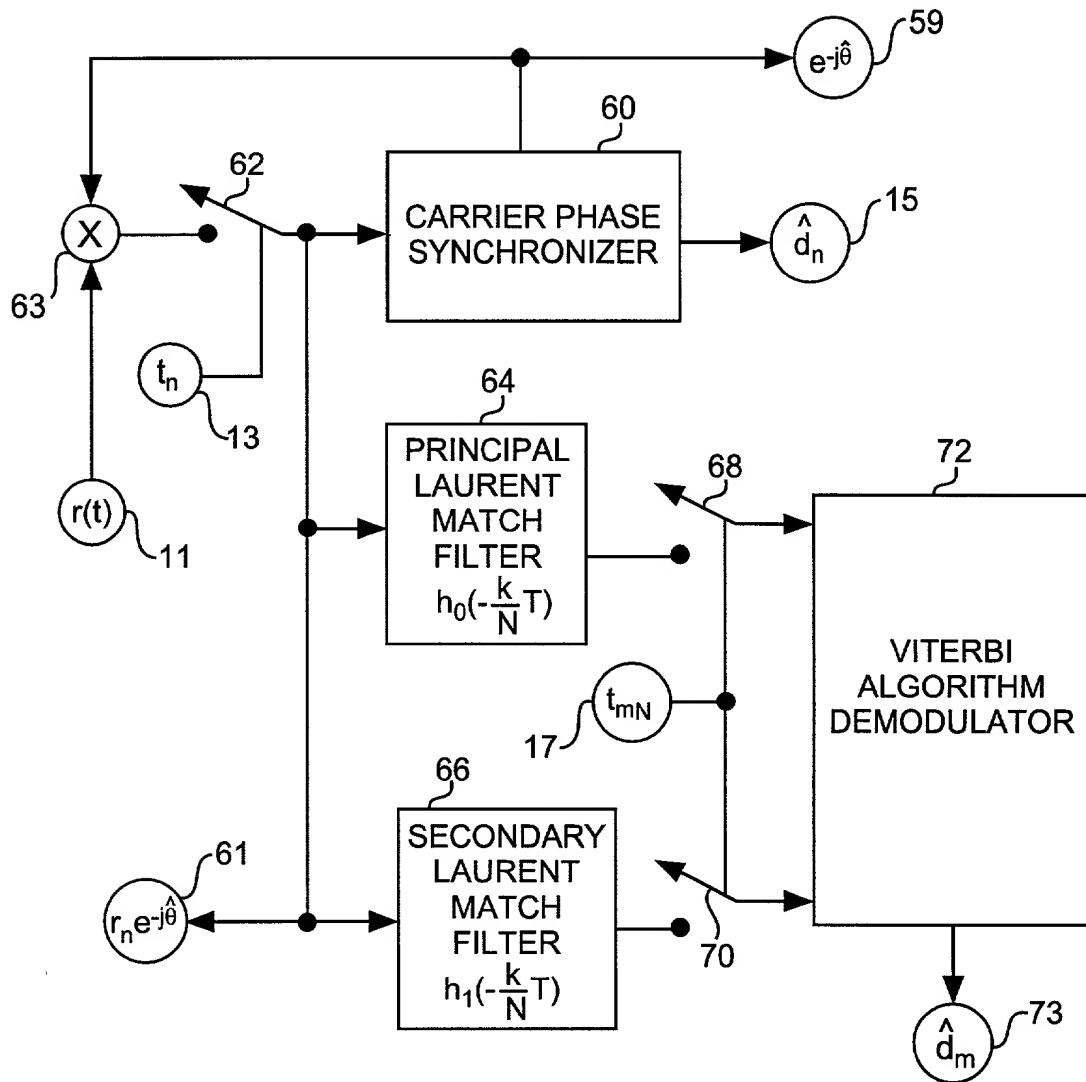
Data aided carrier phase and symbol timing synchronizers are easily implemented at baseband in digital loops for providing reliable data demodulation from noisy received signals having dynamic carrier phase and symbol timing errors as found in continuous phase modulation communications systems such as Gaussian minimum shift keying systems. Both the symbol time and carrier phase synchronizers can be used in a signal demodulation system.

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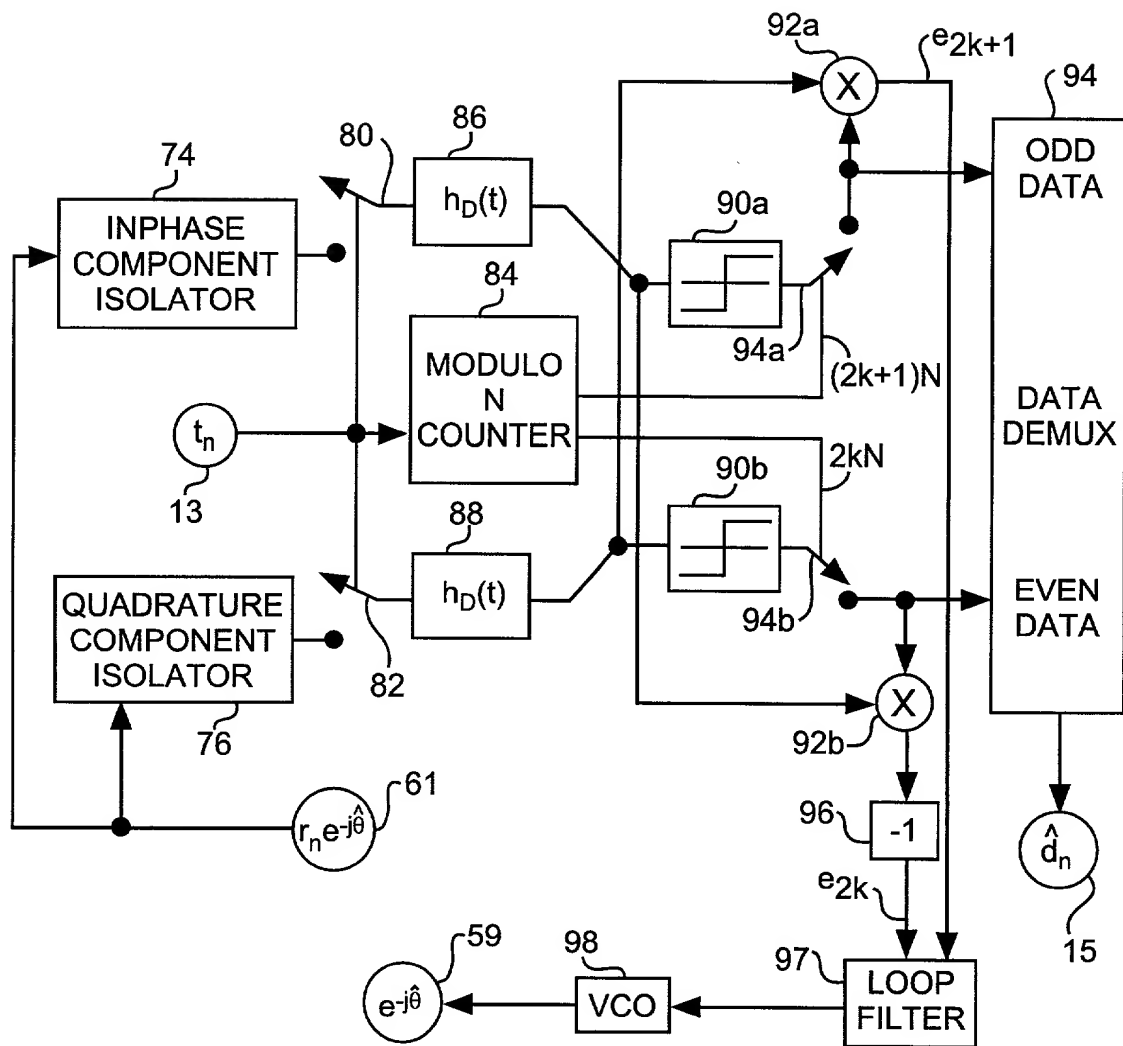
SYMBOL TIME SYNCHRONIZED DATA DEMODULATOR

FIG. 1A



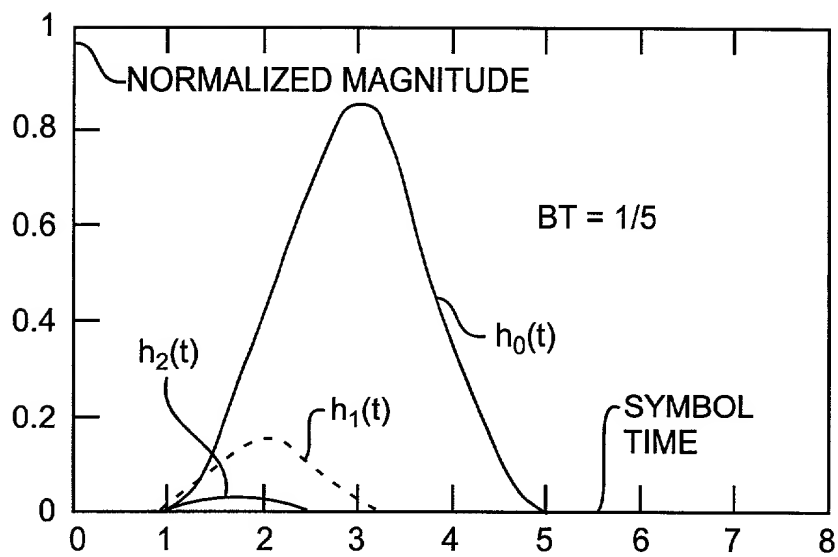
CARRIER PHASE SYNCHRONIZED DATA DEMODULATOR

FIG. 2A



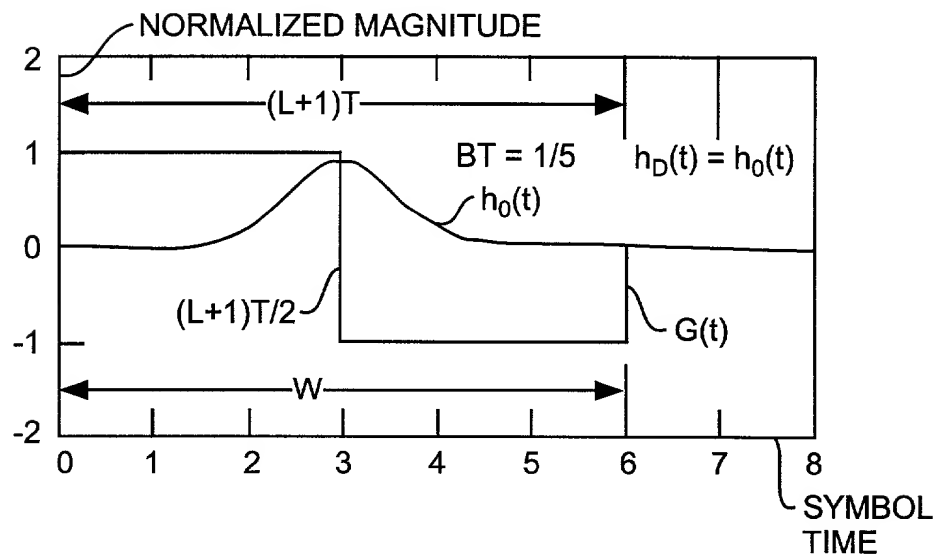
CARRIER PHASE SYNCHRONIZER

FIG. 2B



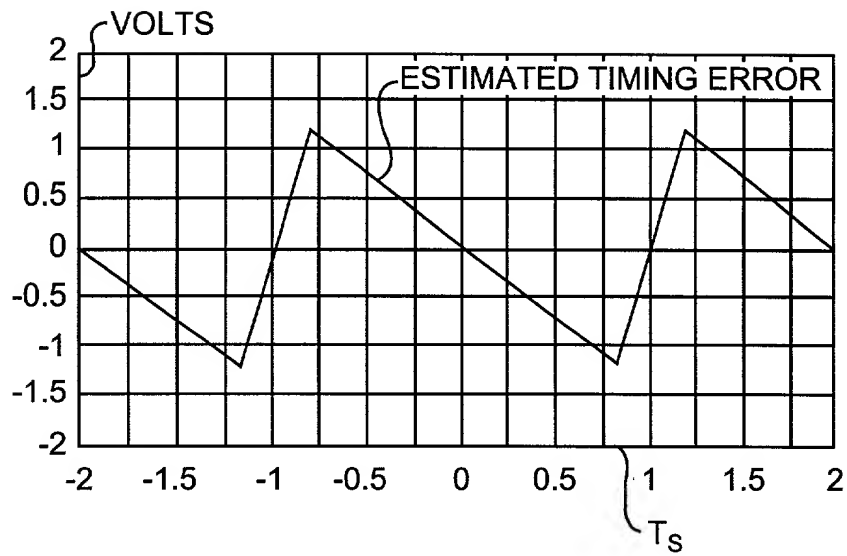
LAURENT PULSE FUNCTIONS

FIG. 3



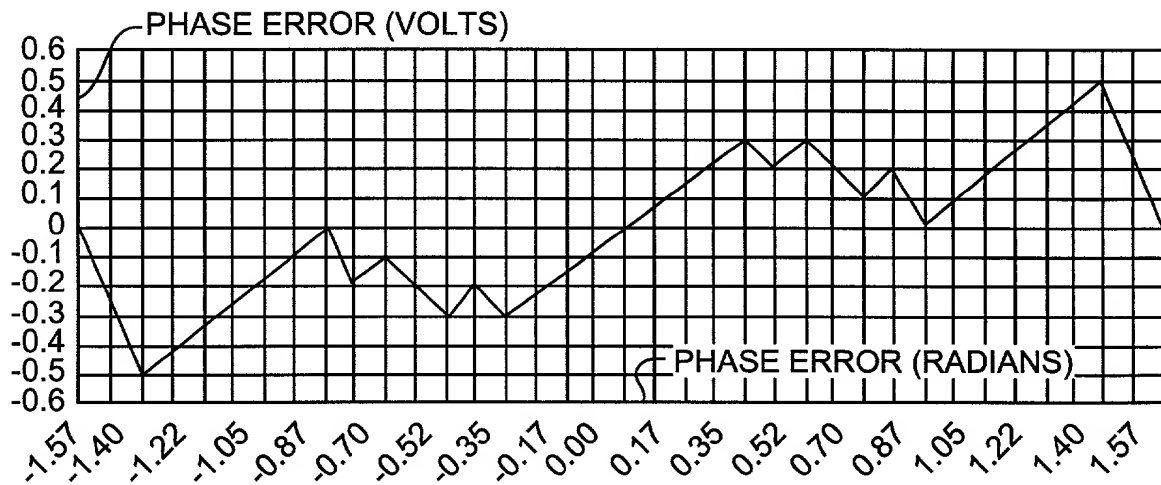
EARLY-LATE GATE FUNCTION

FIG. 4



SYMBOL TIMING ERROR DISCRIMINATOR CURVE

FIG. 5



CARRIER PHASE ERROR DISCRIMINATOR CURVE

FIG. 6

PATENT

Attorney's Docket No. D-387

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is of the following type:

/X/ original

INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

Data Aided Symbol Timing Tracking System for Precoded Continuous Phase Modulated Signals

SPECIFICATION IDENTIFICATION

The specification of which is attached hereto.

ACKNOWLEDGEMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations section 1.56(a).

/x/ In compliance with this duty there is attached an information disclosure statement. 37 CFR 1.97.

POWER OF ATTORNEY

As a named inventor, I hereby appoint the following attorney(s) and/or agents(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

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DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

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Inventor's signature: 

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Full name of third joint inventor, if any: _____

Inventor's signature: _____

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Full name of fourth joint inventor, if any: _____

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